Investigate and Reduce Capacitive Couplings in a Flyback Adapter With a DC-Bus Filter to Reduce EMI

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***Abstract*—In consumer electronics, high power density power adapters are designed to minimize the adapter size. As a result, the components are getting very close and the near-field coupling issue tends to be severe. This compromises the performance of electromagnetic interference filters, especially at high frequencies. This article investigates near-field capacitive couplings and the reduction techniques in a high power-density power adapter with a dc-bus filter. The parasitic capacitive coupling theory is developed and parasitic coupling capacitances are experimentally extracted. The common-mode (CM) noise model with parasitic capacitive couplings is developed and the techniques to reduce the CM noise due to parasitic capacitive couplings are explored. Simulation and experiments were conducted to verify the analysis and the proposed techniques.**

***Index Terms*—Active clamp Flyback converter, capacitive coupling, dc-bus filter, parasitic capacitance cancellation, shielding.**

I. Introduction

INCREASING the switching frequency of power converters helps to increase their power density. However, high switching frequency can cause severe high-frequency (HF) electromagnetic interference (EMI) noise. Therefore, EMI filters with good HF performance are desired in the high power-density power converter design.

Near-field coupling has been identified as a significant factor that limits the HF performance of EMI filters [1]. In consumer electronics, the components in high power-density ac/dc power adapters are very close to each other, so the near-field coupling could be significant. Moreover, in order to improve power efficiency, in some designs, the EMI filter is located on dc bus [8] instead of on ac line. It will be discussed in this article later that dc-bus filters tend to have capacitive coupling issues.

Conventionally, there are two different near-field couplings: inductive coupling and capacitive coupling. Many literatures focus on the analysis and reduction of inductive couplings [1]–[4], [21]–[29] including those between two equivalent series inductances (ESL) of a pair of capacitors [1], [2], between a filter inductor and a capacitor's ESL [1], [3], between a capacitor's ESL and its adjacent printed-circuit-board (PCB) trace loop [1], [29] and between two PCB trace loops [1], [4]. For EMI filters with multiple components, the couplings could be complicated. In [1], [2], [23], [25], and [27], the inductive couplings in a *CLC* π-filter are identified and reduced. In [21], [26], and [28], the couplings in an *LCL* T-filter are analyzed. For more complicated filter structures, three-dimensional finite-element analysis can help to extract the parasitic coupling parameters in an EMI filter [22], [23], [26].

On the other hand, not many literatures address the capacitive coupling. In [5], the capacitive coupling between the metal foils of two bulk capacitors is identified. However, the techniques to extract and reduce the parasitic capacitance were not further investigated. In [6], [21], [28], and [30], the capacitive couplings due to the PCB traces across an *LCL* T-filter are explored. In order to mitigate the couplings, PCB slits and shielding are applied to reduce and bypass the noise current [6], [21], [31], [33]. The technique was verified within a filter, but the performance when used in a converter was not presented.

In [7], the capacitive coupling between the PCB traces across an inductor is investigated by the same authors of this article. By improving the PCB layout or applying the parasitic capacitance cancellation technique, the capacitive coupling can be greatly reduced. The techniques are going to be further explored and improved in this article. Also, in the existing literatures, the investigation focuses on the capacitive coupling among components carrying low noise voltages. In this article, it is found that the capacitive coupling between the conductors or components with high pulsating voltages and sensitive nodes could be more important.

This article is organized as follows. In Section II, the common-mode (CM) noise models of an active-clamp Flyback adapter with an ac-line or a dc-bus EMI filter are developed and compared without any capacitive couplings included. The CM noise of the converter with an ac-line or a dc-bus EMI filter is also measured and compared. In Section III, the capacitive couplings are identified and the coupling mechanism is studied. The parasitic coupling parameters are also extracted for the development of the CM noise model. In Section IV, different capacitive coupling reduction techniques, such as parasitic capacitance cancellation

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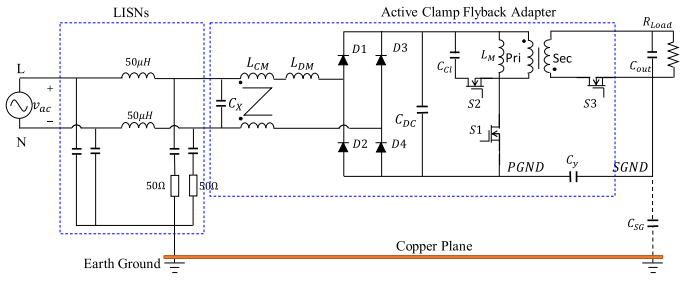

Fig. 1. AC/DC active clamp Flyback adapter with an ac-line filter.

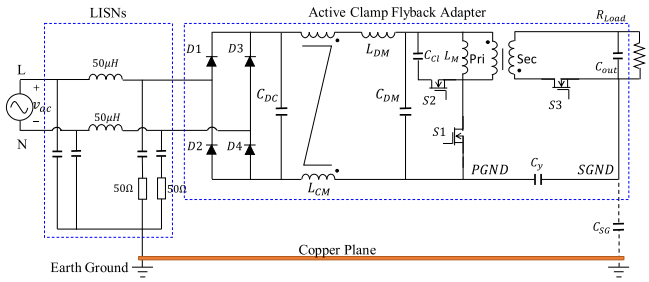

Fig. 2. AC/DC active clamp Flyback adapter with a dc-bus filter.

and shielding techniques, are investigated to reduce the CM EMI due to capacitive couplings. Simulation and experiments were conducted to verify the proposed techniques.

II. CM Noise Models of an Active Clamp Flyback Adapter With an AC-Line or DC-Bus Filter

A. Active Clamp Flyback Adapters With an AC-Line or DC-Bus Filter

Fig. 1 shows an active clamp Flyback adapter with a conventional ac-line EMI filter line impedance stabilization networks (LISNs). The low-line and high-line input voltages are 120-V/60-Hz ac and 240-V/50-Hz ac, respectively. The output voltage is 20-V dc, and the output power is 65 W. The converter has a switching frequency of 150 kHz. S_2 and $C_{\rm Cl}$ are active clamp components used to improve converter's power efficiency. A CM inductor $L_{\rm CM}$(700 μH) with two fully coupled windings is placed at the ac input and a Y-capacitor C_y(470 pF) is placed across the primary ground (PGND) and secondary ground (SGND) to reduce the CM EMI noise. An *LC* filter, which is composed of a differential-mode (DM) inductor $L_{\rm DM}$(300 μH) and an X-capacitor C_X(0.47 μF) on ac line, reduces the DM EMI noise. The SGND of the adapter is floating. $C_{\rm SG}$ represents the parasitic capacitance between SGND and the earth ground. $C_{\rm SG}$ is measured as around 10 pF.

Because the diode bridge turns ON/OFF at 50/60 Hz, the ac input current of the adapter has large line-frequency current ripples, which result in a large root mean square (rms) and peak current. Therefore, the winding power loss of the CM and DM inductors could be significant. Furthermore, the X-capacitor C_X needs to meet the ac-line safety requirement EN60950. Therefore, a film capacitor should be used. The film capacitor has large size due to its low permittivity. In order to improve the power efficiency and power density of the adapter, a dc-bus filter [8] can be applied in Fig. 2. In Fig. 2, the EMI filter is moved from ac line to dc bus. Since the ac-line current ripple due to the diode bridge is mostly filtered out by the bulk electrolytic capacitor $C_{\rm DC}$(82 μF), the current flowing through the inductors $L_{\rm CM}$ and $L_{\rm DM}$ is almost a constant dc current. Since the peak current in a dc-bus inductor is greatly reduced, the DM inductor is to be saturated at a higher current than an ac-line inductor. Therefore, a smaller magnetic core can be used for $L_{\rm DM}$. Also, the rms current in a dc-bus inductor is smaller than that in an ac-line inductor, so the winding power loss in a dc-bus inductor is smaller than that of an ac-line inductor. Moreover, ceramic capacitors can be used as the DM capacitance $C_{\rm DM}$(0.47 μF) without the limitation of the same safety standard as required for ac-line filters. Due to its high permittivity, the size of ceramic capacitors on dc bus is much smaller than that of film capacitors on ac line even the capacitance derating due to dc-bus voltage bias is considered.

TABLE I
Comparison of the Size and Power Loss of an AC-Line Filter and a DC-Bus Filter in a 65-W Flyback Adapter

EMI Filter Components		Characteristics of Filter Components		
		Value	Size (mm^3)	Loss[a] (mW)
AC Line	Ferrite Toroid Core:L_{CM}	L=700 μH DCR=203 mΩ	120	292
	High Flux Core:L_{DM}	L=300 μH DCR=383 mΩ	1370	552
	Safety Film Capacitor:C_X	C=0.47 μF ESR=20 mΩ	2900	<1
	Total		4390	844
DC Bus	Ferrite Toroid Core:L_{CM}	L=700 μH DCR=203 mΩ	120	32.5
	High Flux Core:L_{DM}	L=300 μH DCR=160 mΩ	435	25.6
	Cermaic Capacitor:C_{DM}	C=0.47 μF*2[b] ESR=20 mΩ/2	71.3*2	10.3
	Total		698	68.4

[a]The power loss is calculated when the input voltage is 120-V ac and the output is 65 W (full load).
[b]When using a ceramic capacitor with dc bus bias voltage, a 50% capacitance derating is needed based on the guideline on the datasheet. So, in actual design, two parallel 0.47-μF capacitors are used.

In order to show the advantages of the dc-bus filter, the size and power loss of the inductors and capacitors in an ac-line filter are compared with those in a dc-bus filter for a 65-W Flyback adapter in Table I. In Table I, by employing a dc-bus filter, the EMI filter size reduces by 84% and the power loss reduces by 775 mW, which indicates the adapter has more than 1% efficiency improvement. The dc-bus filter is, therefore, preferred for many high power-density designs.

B. CM Noise Model for Active Clamp Flyback Adapters

For CM noise analysis in the conducted EMI frequency range from 150 kHz to 30 MHz, the impedances of the line and neutral of the ac power line between the diode bridge and LISNs can be ignored. It is assumed that the CM impedance of LISNs is approximately 25 Ω [9] within the conducted EMI range. The CM inductance of the coupled CM inductor $L_{\rm CM}$ is equal to the single winding's inductance $L_{\rm CM}$. The impedance of the diode bridge can be ignored [11] even when it is OFF for CM EMI

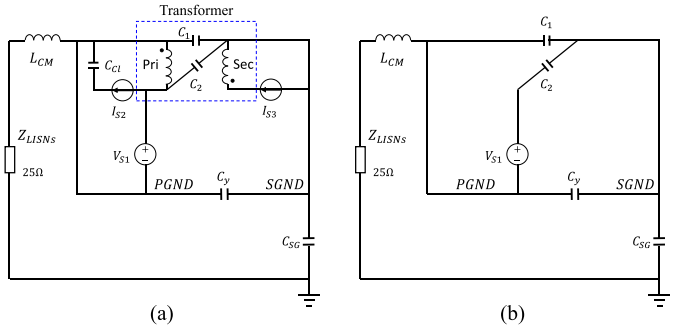

Fig. 3. (a) CM noise model with the substitution theory applied. (b) CM noise model with the superposition theory applied.

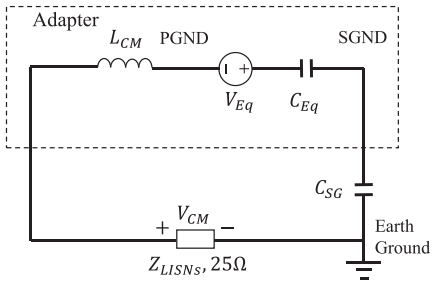

Fig. 4. Final CM noise model of an active clamp Flyback adapter.

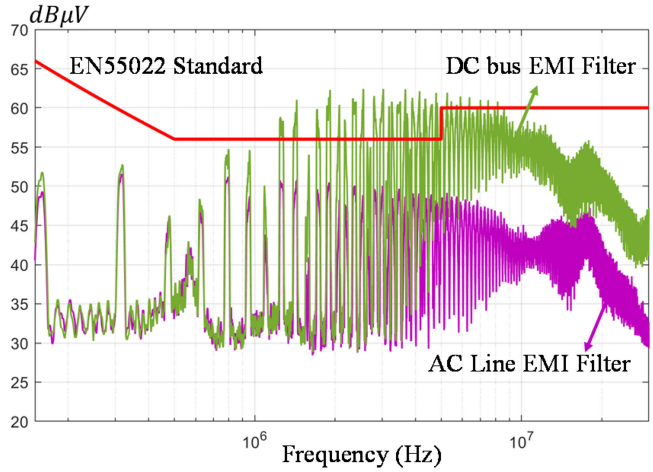

Fig. 5. Measured CM EMI noise of Flyback adapters with an ac-line filter or a dc-bus filter.

analysis because its 50-pF junction capacitance is much larger than $C_{\rm SG}$. The equivalent series resistance (ESR) and the ESL of the bulk capacitor $C_{\rm DC}$ is 0.8 Ω and 20 nH, respectively. Because of this, the impedance of $C_{\rm DC}$ is below 5 Ω in the conducted EMI range, which is much smaller than the impedance of $L_{\rm CM}$ or $C_{\rm SG}$, so $C_{\rm DC}$ can be considered as short circuit for EMI analysis. Similarly, C_X (ESR = 20 mΩ, ESL = 2.5 nH) in Fig. 1, $C_{\rm DM}$ (For a single 0.47-μF ceramic capacitor, ESR = 20 mΩ, ESL = 1.5 nH) in Fig. 2, and the output capacitor $C_{\rm out}$ (ESR = 8 mΩ, ESL = 5 nH) can also be considered as short circuit for EMI analysis [9].

In Figs. 1 and 2, based on the substitution theory, S1 can be replaced with a voltage source V_{S1}, which has the same voltage waveform as the MOSFET drain-to-source voltage; S2 and S3 can be replaced with current sources I_{S2} and I_{S3}, which have the exact same current waveforms as the MOSFET currents [13]. Another important component in the CM noise analysis is the transformer which is a four-port component. Thanks to the research in [12], the transformer's interwinding parasitic capacitance can be represented with a two-capacitor model for CM noise analysis. The impedance of $L_{\rm DM}$ can be ignored in the CM noise analysis because of the full coupling between $L_{\rm CM}$'s two windings. Based on the aforementioned analysis, the circuit in Figs. 1 and 2 can be represented with the model shown in Fig. 3(a).

The superposition theory can be applied to simplify the model in Fig. 3(a). Based on the superposition theory, the effect of a voltage/current source on CM EMI can be analyzed by shorting other voltage sources and disconnecting other current sources. Based on this, it was found that, only the noise generated by V_{S1} flows through LISNs [10]. As a result, I_{S2} and I_{S3} can be removed from the model. Furthermore, both transformer windings are in parallel with the voltage source V_{S1}, thus, they can be removed, as shown in Fig. 3(b). Based on the transformer capacitance extraction technique introduced in [12], C_1 and C_2 are extracted as 107 pF and −2.1 pF. It should be noted that C_2 is an equivalent capacitance in the transformer model and its value can be either positive or negative [10], [12]. The transformer has been optimized for the CM noise reduction based on the transformer design technique in [10], so C_2 is small.

Based on the Thevenin equivalence, the circuit between PGND and SGND can be modeled with an equivalent capacitance $C_{\rm Eq}$ and an equivalent voltage source $V_{\rm Eq}$ in (1) and (2). The final model is shown in Fig. 4. $V_{\rm CM}$ is the CM voltage drop on LISNs. It should be noted that the CM noise models for the circuits in Figs. 1 and 2 are identical, which indicates that theoretically, the location of the EMI filter, either on the ac-line side or dc-bus side, does not change the CM noise model.

$$V_{\rm Eq} = \frac{C_2}{C_1 + C_2 + C_y} V_{S1} \tag{1}$$

$$C_{\rm Eq} = C_1 + C_2 + C_y. \tag{2}$$

C. CM Noise of Power Adapters With an AC-Line or DC-Bus Filter

The CM EMI noise of power adapters with an ac-line or a dc-bus EMI filter was measured in Fig. 5. The input voltage is 240-V ac, which represents the worst case for the CM EMI noise since the switching voltage V_{S1} is the highest. In the measurement, all component values in two adapters are identical. The model in Fig. 4 does not include any parasitic couplings. Based on this model, the CM noise should be equal for the two adapters. However, in Fig. 5, the adapter with an ac-line filter meets the conducted EMI standard, whereas the CM noise of the adapter with a dc-bus filter is 15 dB higher than the noise with the ac-line filter at high frequencies. It is higher than the EMI standard EN55022. It indicates there are issues that have not been identified and investigated for the dc-bus filter implementation.

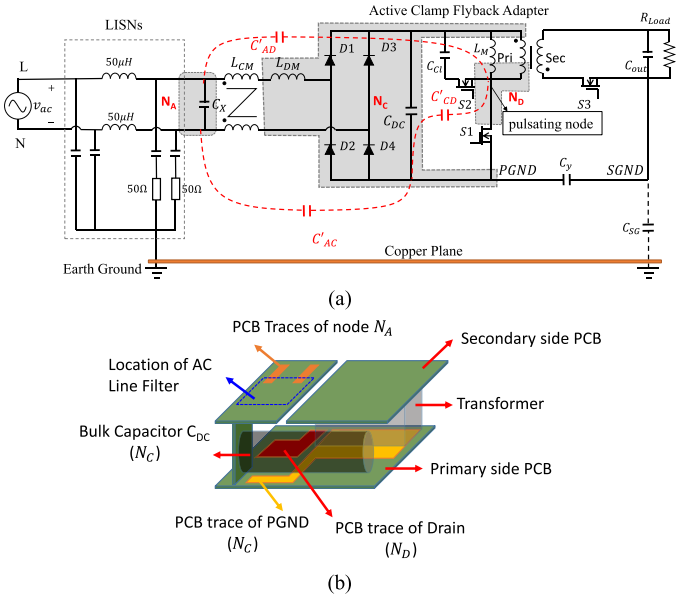

Fig. 6. (a) Voltage nodes and capacitive couplings in an ac/dc active clamp Flyback adapter with an ac-line filter and LISNs. (b) Physical layout.

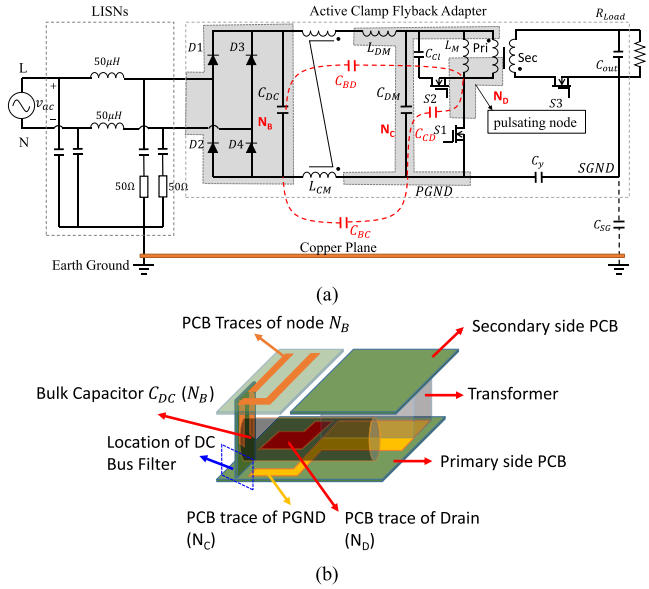

Fig. 7. (a) Voltage nodes and capacitive couplings in an ac/dc active clamp Flyback adapter with a dc-bus filter and LISNs. (b) Physical layout.

III. Identification and Analysis of the Near-Field Capacitive Couplings

A. Capacitive Couplings in an Active Clamp Flyback Converter With an AC-Line Filter

The undesired capacitive couplings usually happen between conductors with different voltages, especially between the sensitive nodes and noisy nodes. In order to identify the capacitive couplings of the converter in Fig. 1, voltage nodes are identified as shaded areas in Fig. 6(a). The adapter's physical layout is in Fig. 6(b). In Fig. 6, node N_A is between the EMI filter and the LISNs on the ac line. The diode bridge, DM inductor $L_{\rm DM}$, bulk electrolytic capacitor $C_{\rm DC}$, and dc-bus PCB traces can be defined as node N_C for the convenience of noise analysis although the diode may not be always ON. As analyzed previously, for CM noise, because of the fully coupled two windings on $L_{\rm CM}$, $L_{\rm DM}$ almost has no voltage drop, so it is included in N_C. Node N_D is the voltage pulsating node. It includes not only the connection between the transformer and the drain of the MOSFET S1 but also the effects of the transformer primary winding as it has gradient and time-varying voltages.

In Fig. 6, node N_A is at the output of the EMI filter, so the noise at N_A should be very low. Any significant capacitive couplings from the noisy nodes to N_A may significantly increase the noise at N_A. Because of this, N_A is identified as sensitive node. On the other hand, node N_D is identified as noisy node. Node N_C includes PGND, so the capacitive coupling $C'_{\rm CD}$ from the node N_D to N_C is equivalently in parallel with MOSFET S1, as a result, it does not contribute to the CM noise on LISNs. On the other hand, the capacitive coupling $C'_{\rm AC}$ between the node N_C and N_A can reduce the performance of the EMI filter, so it is important. Similarly, the capacitive coupling $C'_{\rm AD}$ between the noisy node N_D and sensitive node N_A is also important if the coupling effect is significant. The induced current $i'_{\rm AD}(s)$ due to $C'_{\rm AD}$ can be approximated as

$$i'_{\rm AD}(s) \approx sC'_{\rm AD}V_{S1}(s) \tag{3}$$

where $V_{S1}(s)$ is the drain-to-source voltage of S1, as shown in Fig. 3. A detailed analysis on this approximation will be given in Section III-D. From (3), the induced current is proportional to $C'_{\rm AD}$.

B. Capacitive Couplings in an Active Clamp Flyback Converter With a DC-Bus Filter

For the active clamp Flyback converter with a dc-bus filter in Fig. 2, the voltage nodes are identified in Fig. 7(a). The adapter's physical layout in Fig. 7(b) is similar to that in Fig. 6(b) for the ac-line filter case. Node N_B includes bulk capacitor $C_{\rm DC}$, the diode bridge and the PCB traces connected to them. It is the output of the EMI filter, so it is a sensitive node. Node N_C includes the DM capacitor $C_{\rm DM}$ and $L_{\rm DM}$ and the PCB traces connected to them. Similar to that in Fig. 6, $L_{\rm DM}$ is included in the node N_C because it almost has no voltage drop for the CM current due to the full coupling between the two windings of $L_{\rm CM}$. The node N_D is a voltage pulsating node same as in Fig. 6.

There are capacitive couplings $C_{\rm BD}$, $C_{\rm BC}$, and $C_{\rm CD}$ between any two nodes. Different from the active clamp Flyback converter with an ac-line EMI filter in Fig. 6, bulk electrolytic capacitor $C_{\rm DC}$ is now in the sensitive node. Any capacitive couplings to $C_{\rm DC}$ could be significant due to its large size. $C_{\rm BC}$ is the parasitic capacitance between the node N_B and N_C. The coupling between the electrolytic capacitor $C_{\rm DC}$ and node N_C may contribute to a big part of $C_{\rm BC}$ because of the small distance between $C_{\rm DC}$ and PGND in Fig. 7(b). $C_{\rm CD}$ can be ignored as it is in parallel with MOSFET S1. $C_{\rm BD}$ is the capacitive coupling between the voltage pulsating node N_D and node N_B. It could be significant due to the large size of the electrolytic capacitor $C_{\rm DC}$. Similar to (3), the induced current $i_{\rm BD}(s)$ due to $C_{\rm BD}$ can

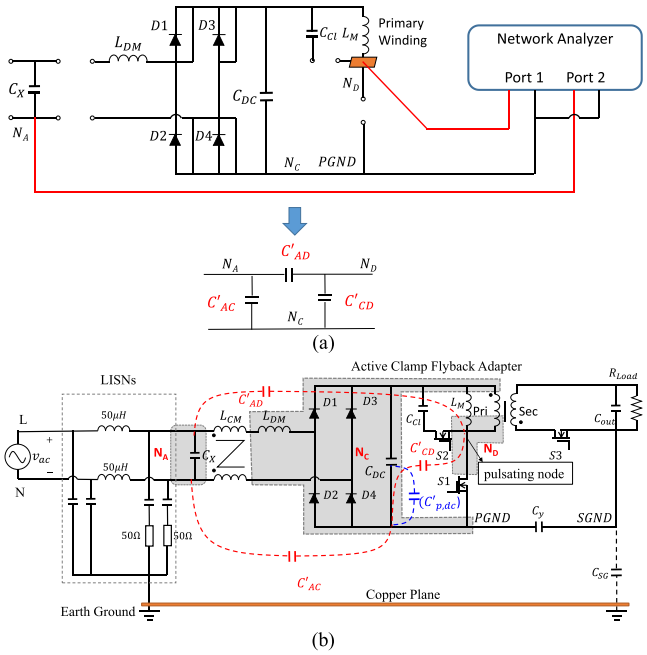

Fig. 8. (a) Measurement setup for $C'_{\rm AC}$, $C'_{\rm AD}$, and $C'_{\rm CD}$. (b) Parasitic capacitance $C'_{\rm p,dc}$ between the metal shell of the electrolytic capacitor $C_{\rm DC}$ and PGND does not contribute to CM noise.

be derived as

$$i_{\rm BD}(s) \approx sC_{\rm BD}V_{S1}(s). \tag{4}$$

From (4), the induced current is proportional to $C_{\rm BD}$.

C. Measurement and Analysis of the Capacitive Couplings

For the Flyback converter with an ac-line filter in Fig. 6, $C'_{\rm AC}$, $C'_{\rm AD}$, and $C'_{\rm CD}$ can be extracted using a vector network analyzer (VNA) in Fig. 8(a) based on the technique in [17]. In Fig. 8(a), the two-port S-parameters is measured with N_C as reference, N_A and N_D as two ports. The π capacitance network can be derived from the measured S-parameters and all three capacitances can be extracted. It should be pointed out that, the contribution of the gradient voltage on the transformer primary winding to $C'_{\rm AD}$ has been included in the measurement as the voltage excitation on the port 1 is added to the transformer primary winding and this voltage is a gradient voltage on the primary winding. $C'_{\rm AC}$ is extracted as 1.9 pF. Compared with the 1-pF equivalent parallel winding capacitance (EPC) and 2.6-kΩ equivalent parallel resistance (EPR) of $L_{\rm CM}$, $C'_{\rm AC}$ has limited influence to $L_{\rm CM}$'s HF performance. Because of the long distance between N_A and N_D in Fig. 6(b), the $C'_{\rm AD}$ is extracted as only 0.026 pF. As the magnitude of V_{S1} at the fundamental switching frequency is around 300 V, based on (3), the induced CM current $i'_{\rm AD}(s)$ is 7.4 μA at the fundamental switching frequency. If all of this current flows through LISNs, the voltage drop on 25-Ω LISNs is 44 dBμV. It is much smaller than the EMI limit EN55022 (66 dBμV for quasi-peak), so its effect can be ignored. As stated previously, $C_{\rm DC}$ is an electrolytic capacitor that has a big metal shell equivalently connected to its negative terminal for the EMI noise as the capacitance between the metal shell and the negative terminal is measured as 0.8 μF. Part of $C'_{\rm AC}$ and $C'_{\rm CD}$ is due to $C_{\rm DC}$'s metal shell. In the physical layout in

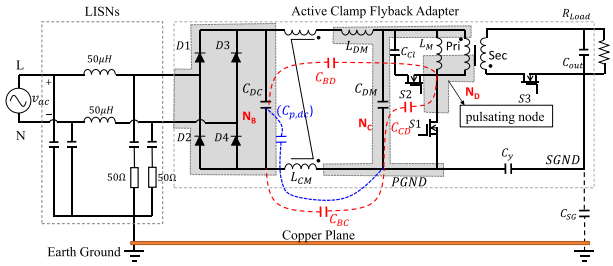

Fig. 9. Parasitic capacitance $C_{\rm p,dc}$, which is part of $C_{\rm BC}$, between the metal shell of the electrolytic capacitor $C_{\rm DC}$ and PGND degrades $L_{\rm CM}$'s performance.

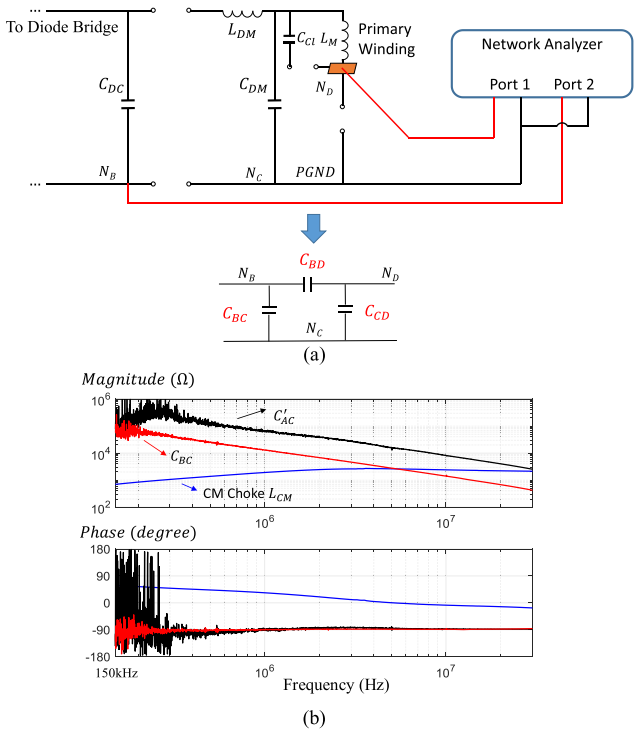

Fig. 10. (a) Measurement setup for $C_{\rm BC}$, $C_{\rm BD}$, and $C_{\rm CD}$. (b) Comparison of the measured impedances of the CM inductor $L_{\rm CM}$, $C'_{\rm AC}$, and $C_{\rm BC}$.

Fig. 6(b), capacitor $C_{\rm DC}$ is right on the PGND copper plane, so there is a large parasitic capacitance $C'_{p,\rm dc}$ between the metal shell and the PGND in Fig. 8(b), but it does not contribute to CM noise.

On the other hand, for the active clamp Flyback converter with a dc-bus filter, with the layout as in Fig. 7(b), because the parasitic capacitance $C_{p,\rm dc}$ between $C_{\rm DC}$ and PGND is significant, it greatly contributes to $C_{\rm BC}$ as in Fig. 9. $L_{\rm CM}$'s performance is thus greatly degraded. Fig. 10 shows the measurement setup for $C_{\rm BC}$, $C_{\rm BD}$, and $C_{\rm CD}$, and the comparison of the measured impedance curves for $C'_{\rm AC}$, $C_{\rm BC}$, and CM inductor $L_{\rm CM}$. In Fig. 10(a), the two-port S-parameters is measured with N_C as reference and N_B and N_D as two ports. Similar to the case with an ac-line filter, the contribution of the gradient voltage on the transformer primary winding to $C_{\rm BD}$ has been included in the measurement as the voltage excitation on the port 1 is added to the transformer primary winding as a gradient voltage. The π capacitance network can be derived from the measured S-parameters and all three capacitances can be extracted. The

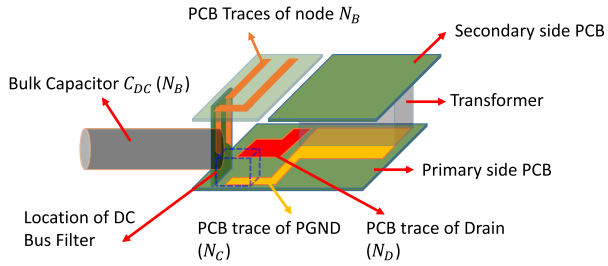

Fig. 11. Place the bulk capacitor away from the primary-side PCB.

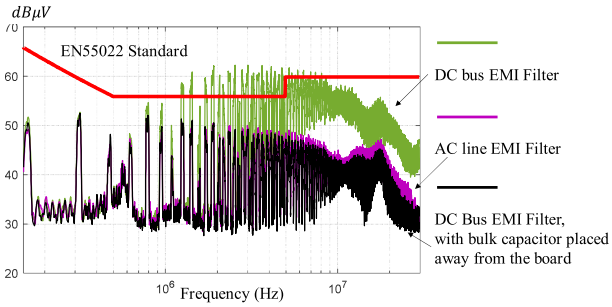

Fig. 12. Comparison of the CM noise of the adapter with the bulk capacitor placed away from the primary-side board and the original CM noise.

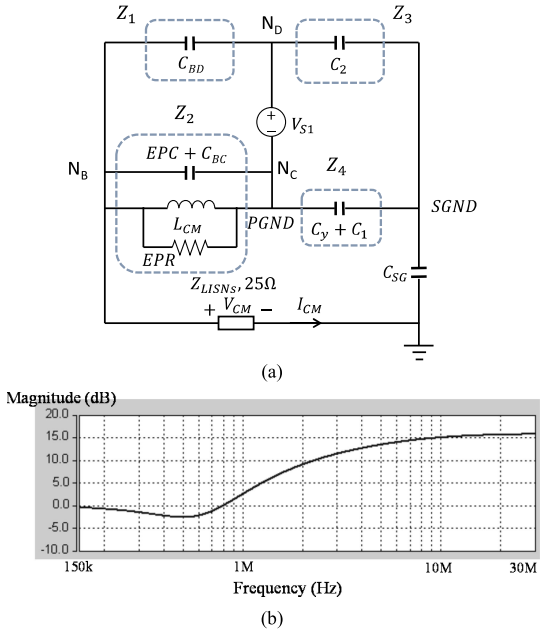

Fig. 13. (a) CM equivalent circuit with a dc-bus filter and capacitive couplings. (b) Simulated difference of the voltage transfer gains of the dc-bus and the ac-line filters.

extracted $C_{\rm BC}$ is 10.4 pF. The noise below 400 kHz in Fig. 10(b) is due to the background noise as the magnitude of signal is too small below 400 kHz. In Fig. 10(b), comparing with 1.9 pF $C'_{\rm AC}$ in the ac-line filter case, 10.4-pF $C_{\rm BC}$ can reduce the impedance $L_{\rm CM}$ above 5 MHz. $C_{p,\rm dc}$ is also extracted as 9 pF that contributes to the most of $C_{\rm BC}$. When extracting $C_{p,\rm dc}$, $C_{\rm DC}$ is disconnected from the circuit but keeps at the same position. $L_{\rm CM}$ and the PCBs at the left side of $C_{\rm DC}$ are also removed [the top left and the vertical boards in Fig. 7(b)]. The distance between $C_{\rm DC}$ and the PGND is kept unchanged. The capacitance between the negative terminal $C_{\rm DC}$ and PGND is measured as $C_{p,\rm dc}$. It should be noted that the location of $C_{\rm DM}$ has little influence on $C_{\rm BC}$ since the size of $C_{\rm DM}$ is very small. The measured capacitance between $C_{\rm DM}$ and $C_{\rm DC}$ when they are adjacent to each other is only 0.3 pF, so it can be ignored compared to $C_{\rm BC}$.

Different from the $C'_{\rm AD}$ in Fig. 6, $C_{\rm BD}$ cannot be ignored because it is much larger than $C'_{\rm AD}$ due to the parasitic capacitance between the big metal shell of $C_{\rm DC}$ and node N_D. The extracted $C_{\rm BD}$ is 0.31 pF. Based on (4), the induced CM current $i_{\rm BD}(s)$ due to $C_{\rm BD}$ is 88 μA at the fundamental switching frequency. If all of this current flow through LISNs, its voltage drops on 25-Ω LISNs is 66 dBμV. It reaches the EMI limit EN55022 (66 dBμV for quasi-peak), so its effect cannot be ignored. This conclusion also holds for high-order switching harmonics based on (4).

In order to verify the effects of capacitive couplings due to the large metal shell of $C_{\rm DC}$ on CM noise, an experiment is conducted in Fig. 11. The bulk capacitor $C_{\rm DC}$ was moved away from the PGND by mounting it on the outside of the adapter. Based on the measurements, $C_{\rm BD}$ is greatly reduced from 0.31 to 0.023 pF and $C_{p,\rm dc}$ is greatly reduced from 9 to 0.7 pF. The CM noise is measured and compared with the original power adapters with an ac-line or dc-bus filter in Fig. 12. In Fig. 12, after the $C_{\rm DC}$ was moved far away from PGND, the CM noise with a dc-bus filter is reduced to a level almost the same as that with an ac-line filter and it meets the EMI standard. Despite this, it will be shown later that $C_{\rm BD}$ and $C_{\rm BC}$ actually play inverse roles on the HF CM EMI.

D. CM Noise Analysis With Capacitive Couplings

The CM noise model in Fig. 3(b) for the active clamp Flyback converter with a dc-bus filter can be improved in Fig. 13 with capacitive couplings and $L_{\rm CM}$'s EPR and EPC included.

The circuit in Fig. 13(a) is a Wheatstone bridge with V_{S1} as the source. The actual CM noise flowing through LISNs is due to the unbalance of the Wheatstone bridge [18]. In the bridge, the branch Z_1 is $C_{\rm BD} = 0.31$ pF. The branch Z_2 includes EPC + $C_{\rm BC}$ = 11.4 pF, $L_{\rm CM}$ = 700 μH, and EPR = 2.6 kΩ in parallel. Branch Z_3 is C_2 = –2.1 pF. Branch Z_4 is $C_y + C1$ = 470 pF + 107 pF. Therefore, $|Z_1|$ and $|Z_3|$ are much larger than $|Z_2|$ and $|Z_4|$, respectively. Based on the theory of the Wheatstone bridge with a large impedance ratio [20], the CM noise can be greatly reduced even the bridge is unbalanced. The low-frequency voltage transfer gain $\rm Gain_{LF}$ from $V_{S1}(s)$ to $V_{\rm CM}(s)$ can be derived as

$$\begin{aligned}\mathrm{Gain_{LF}} = \frac{V_{\rm CM}}{V_{S1}} &= \frac{Z_{\rm LISNs}\left(\frac{Z_2}{Z_1+Z_2}-\frac{Z_4}{Z_3+Z_4}\right)}{Z_{\rm LISNs}+Z_{\rm CSG}+\frac{Z_1Z_2}{Z_1+Z_2}+\frac{Z_3Z_4}{Z_3+Z_4}} \\ &\approx \frac{Z_{\rm LISNs}}{Z_{\rm CSG}}\left(\frac{Z_2}{Z_1}-\frac{Z_4}{Z_3}\right) \approx -Z_{\rm LISNs}\frac{sC_{\rm SG}C_2}{C_y+C_1} \quad (5)\end{aligned}$$

where $Z_{\rm CSG}$ is the impedance of $C_{\rm SG}$(10 pF). It should be noted that since $Z_{\rm LISNs}$ (25 Ω) is much smaller than $Z_{\rm CSG}$ in the conducted EMI range, when deriving the CM current $I_{\rm CM}$ flowing through $Z_{\rm LISNs}$, $Z_{\rm LISNs}$ is ignored. This approximation is also applied in the rest of the article.

From (5), LF CM noise is mostly determined by C_2 and C_{SG}. At high frequencies, the impedance of EPC + C_{BC} is smaller than that of L_{CM} and EPR in parallel. As a result, the unbalance and CM noise is determined by all parasitic capacitances in the Wheatstone bridge. The HF voltage transfer gain Gain_{HF} can be derived as

$$\text{Gain}_{HF} = \frac{V_{CM}}{V_{S1}} \approx \frac{Z_{LISN} s \left(\frac{sC_{BD}}{C_{BC}+EPC} - \frac{sC_2}{C_y+C_1} \right)}{\frac{1}{C_{SG}} + \frac{1}{C_{BC}+EPC} + \frac{1}{C_y+C_1}}$$

$$\approx Z_{LISN} s \frac{sC_{SG}C_{BD}}{C_{BC}+EPC+C_{SG}}. \quad (6)$$

In the aforementioned equation, based on the aforementioned extracted capacitances, the bridge is unbalanced (numerator is not zero). The approximation in (6) holds because C_y is much larger than other capacitances. It is shown that for the unbalanced bridge, the HF CM noise is proportional to C_{BD}. On the other hand, increasing C_{BC} actually helps reduce the HF CM EMI. From (6), the HF EMI reduction in Fig. 12 after moving C_{DC} away from the primary-side PCB is, therefore, due to the fact that the reduction of the numerator due to the reduction of C_{BD} is much more than the reduction of the denominator due to the reduction of C_{BC}.

The boundary frequency f_B between low frequencies and high frequencies mentioned previously can be approximately derived based on the analysis of the transfer gain of Fig. 13(a), as follows:

$$f_B \approx \frac{1}{2\pi\sqrt{L_{CM}\sqrt{(EPC+C_{BC}+C_{SG})\left[EPC+C_{BC}-\frac{C_{BD}}{C_2}(C_1+C_y)\right]}}}. \quad (7)$$

Here, f_B is calculated as 890 kHz. In order to validate the derivation from (5) to (7), a simulation is conducted in Saber. The values of the components in the simulation are the same as the extracted in this section. Fig. 13(b) shows the simulated difference between the transfer gains of the dc-bus filter and the ac-line filter based on Fig. 13(a). In the simulation, the transfer gain of the ac-line filter was simulated after changing C_{BD} and C_{BC} in Fig. 13(a) to C'_{AD} and C'_{AC}. In Fig. 13(b), the gain difference between the two filters matches the difference of the measured noise in Fig. 12, which also validated the model and the analysis. It is shown that the dc-bus filter becomes worse after f_B because C_{BD} begins to play a role in the balance of the bridge. Before f_B, the CM noise is mainly determined by transformer parasitics.

IV. Techniques to Reduce CM EMI Due to Capacitive Couplings

A. CM Noise Reduction With Single Shielding Technique

For the active clamp Flyback converter with a dc-bus filter, from (6), if C_{BD} can be eliminated, the HF CM noise can be greatly reduced. In order to eliminate C_{BD}, a copper foil was used in Fig. 14(a) to shield C_{DC} from the node N_D and the PGND copper plane on the PCB. The copper foil is grounded to PGND, so it is part of node N_C. The equivalent circuit with the copper foil shielding is shown in Fig. 14(b). In Fig. 14(b), with the copper shielding applied, there is a parasitic capacitance C_{SD} between node N_D and the shielding (node N_C), and a parasitic

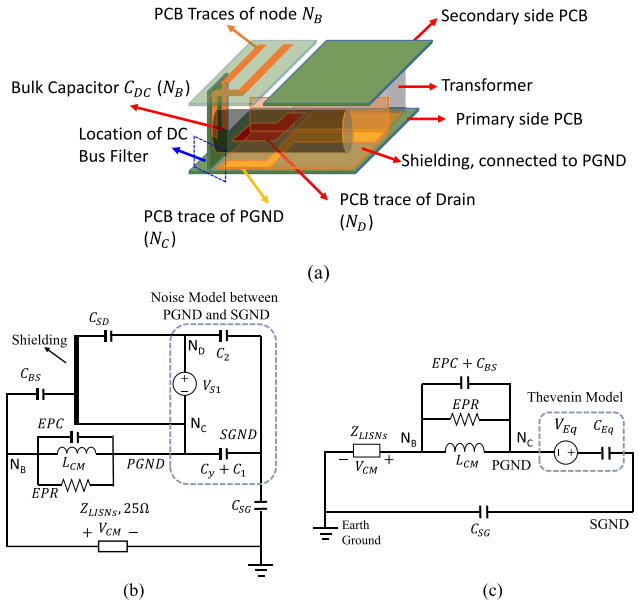

Fig. 14. (a) Apply a copper shielding to reduce the capacitive coupling due to the metal shell of electrolytic capacitor C_{DC}. (b) Equivalent circuit. (c) CM noise model of a power adapter with the copper shielding.

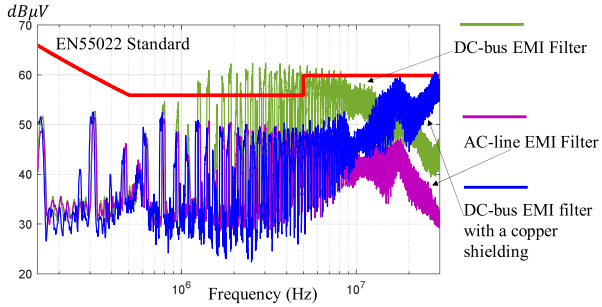

Fig. 15. Measured CM EMI noise with a copper shielding to eliminate the parasitic capacitive coupling between the metal shell of the electrolytic capacitor C_{DC} and node N_D.

capacitance C_{BS} between C_{DC} (node N_B) and the shielding (node N_C). C_{BS} was measured as 30 pF. The C_{BD} in Fig. 13 is equivalently eliminated in Fig. 14(b). C_{SD} does not contribute to CM noise as it is in parallel with V_{S1}.

The equivalent circuit between PGND and SGND is, therefore, similar to the model shown in Fig. 3(b). As a result, Fig. 14(b) is simplified to Fig. 14(c), where V_{Eq} and C_{Eq} are defined in (1) and (2). In Fig. 14(c), it is obvious that C_{BS} + EPC will degrade the CM inductor HF performance. Fig. 15 shows the measured CM EMI noise with the shielding. In Fig. 15, with the copper shielding, the EMI noise between 1 and 12 MHz is reduced by up to 13 dB, and it is close to the EMI performance with an ac-line filter below 10 MHz. The measured CM EMI is still higher than the EMI standard around 16 and 30 MHz due to large C_{BS} based on Fig. 14(b).

B. CM Noise Reduction With Capacitance Cancellation

To further reduce the CM EMI with single shielding technique so as to meet EMI standard at high frequencies, the other

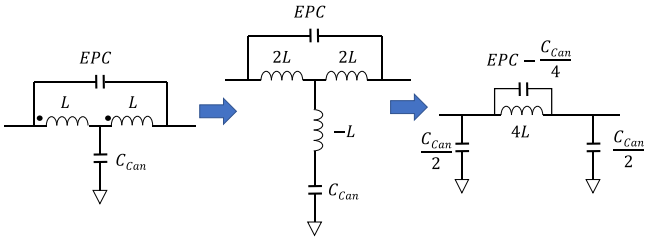

Fig. 16. Winding capacitance EPC cancellation for a CM inductor.

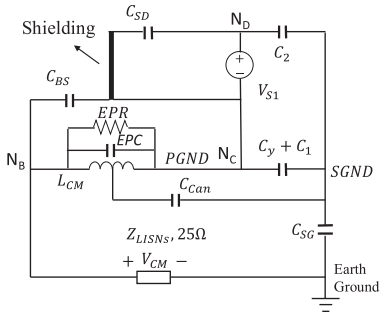

Fig. 17. Improving inductor performance by canceling EPC + $C_{\rm BS}$.

techniques should be explored. In [15], [16], [19], [32], and [34], the parasitic winding capacitance cancellation techniques are proposed to cancel the EPC of an inductor.

Since $C_{\rm BS}$ is parallel to EPC, the winding capacitance cancellation technique can be explored to cancel $C_{\rm BS}$ + EPC in Fig. 14. As shown in Fig. 16, for an inductor with EPC, a cancellation capacitor $C_{\rm Can}$, which is equal to 4EPC is connected between the tap of the two fully coupled windings on the inductor and the ground. The EPC can be canceled because a negative capacitance equal to –EPC is generated in parallel with EPC. The turn ratio of the two windings can be 1:1 or 1:n (if 1:n, the cancellation capacitance would be $(n+1)^2$EPC/n). 1:1 turn ratio can easily achieve high coupling coefficient with the bifilar winding structure, which is critical for HF EPC cancellation and improving CM inductor's HF performance [16], [19], so it will be used here. The issue of applying the technique to $L_{\rm CM}$ is that there is no earth ground in the power adapter to connect $C_{\rm Can}$ when two-prong power plugs are used in these power adapters.

Further investigation on Fig. 16 discloses that $C_{\rm Can}$ is not necessarily connected to the earth ground because as long as $C_{\rm Can}$ is connected to the returning path of the CM noise current, for example, SGND in Fig. 14(b), the cancellation principle still holds. This is because the network transformation in Fig. 16 is still correct even $C_{\rm Can}$ is not connected to the earth ground.

Fig. 17 shows using this cancellation technique to cancel $C_{\rm BS}$ + EPC based on Fig. 14. A cancellation capacitor $C_{\rm Can}$ is connected between the center tap of one winding of the CM inductor and SGND. Fig. 18 shows the equivalent circuit. If $C_{\rm Can}$ is equals to 4(EPC + $C_{\rm BS}$), EPC + $C_{\rm BS}$ is canceled. Because $C_{\rm Can}$ (to discuss later) and $C_{\rm SG}$(10 pF) is much smaller than $C_{\rm Eq}$, which is $C_1 + C_{\rm y} + C_2 = 575$ pF, based on Fig. 18, the voltage transfer gain $\text{Gain}_{\rm Can}$ after EPC + $C_{\rm BS}$ is canceled as

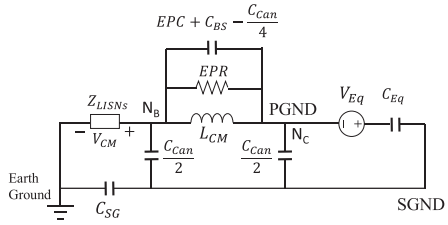

Fig. 18. CM noise model of a power adapter with capacitance cancellation.

given the following equation, where $V_{\rm Eq}$ is defined in (1).

$$\text{Gain}_{\rm Can} = \frac{V_{\rm CM}}{V_{\rm Eq}} \approx \frac{Z_{\rm LISN}sC_{\rm SG}}{C_{\rm SG}+\frac{C_{\rm Can}}{2}} \frac{s\left(C_{\rm SG}+\frac{C_{\rm Can}}{2}\right)\left(\frac{sL_{\rm CM}}{\rm EPR}+1\right)}{s^2\left(C_{\rm SG}+\frac{C_{\rm Can}}{2}\right)L_{\rm CM}+\frac{sL_{\rm CM}}{\rm EPR}+1}. \quad (8)$$

It is shown in Fig. 18 that, with the cancellation technique, EPC + $C_{\rm BS}$ can be canceled. At the same time, the two resultant capacitances $C_{\rm Can}$/2 work as part of the CM filter for the CM noise reduction. Because the two windings of $L_{\rm CM}$ are fully coupled, connecting $C_{\rm Can}$ = 4(EPC + $C_{\rm BS}$) to the center tap of one winding gives the similar performance to that by connecting two $C_{\rm Can}$ = 2(EPC + $C_{\rm BS}$) to the center taps of two windings, respectively, where EPC is the total winding capacitance of the coupled two windings and it is equal to twice of the winding capacitance of one winding.

The circuit realization and analysis of this are shown in Fig. 19(a). As aforementioned, for CM analysis, the two windings of the CM inductor are in parallel. Therefore, the EPC and EPR of two windings are combined for simplification in Fig. 19(a). Due to the symmetrical winding structure, the mutual inductances can be defined as M1 between winding halves in the same winding and M2 or M3 between winding halves in the different windings. A cancellation capacitor is connected to the center tap of one winding. In experiments, a wire is used to connect the capacitor to SGND. The length of the wire is 5 cm and its inductance L_W is measured as 60 nH. The ESL of the cancellation capacitor is only 2 nH, which is much smaller than L_W, therefore, the ESL can be ignored. After decoupling the mutual inductances in Fig. 19(a), it is shown that M2 and M3 will not influence the HF performance of the cancellation, whereas M1 and L_W will. The model in Fig. 19(a) can be further transformed into Fig. 19(b) with a similar method to that in Fig. 16. It is obvious that when the impedance of $L_W + 1/2(\text{L} - \text{M1})$ is much smaller than $C_{\rm Can}$, the cancellation technique works. After the resonance frequency f_r, which is expressed in (9), the cancellation technique will be ineffective.

$$f_r = \frac{1}{2\pi\sqrt{C_{\rm Can}\left[L_w+\frac{1}{2}\left(L-M_1\right)\right]}}. \quad (9)$$

In order to increase M1 so as to increase f_r, a bifilar winding structure is applied in Fig. 19(c) to improve the coupling of the winding halves in the same winding. In Fig. 19(c), the measured L-M1 of the bifilar winding is much smaller than that of the conventional winding structure. Therefore, the HF performance

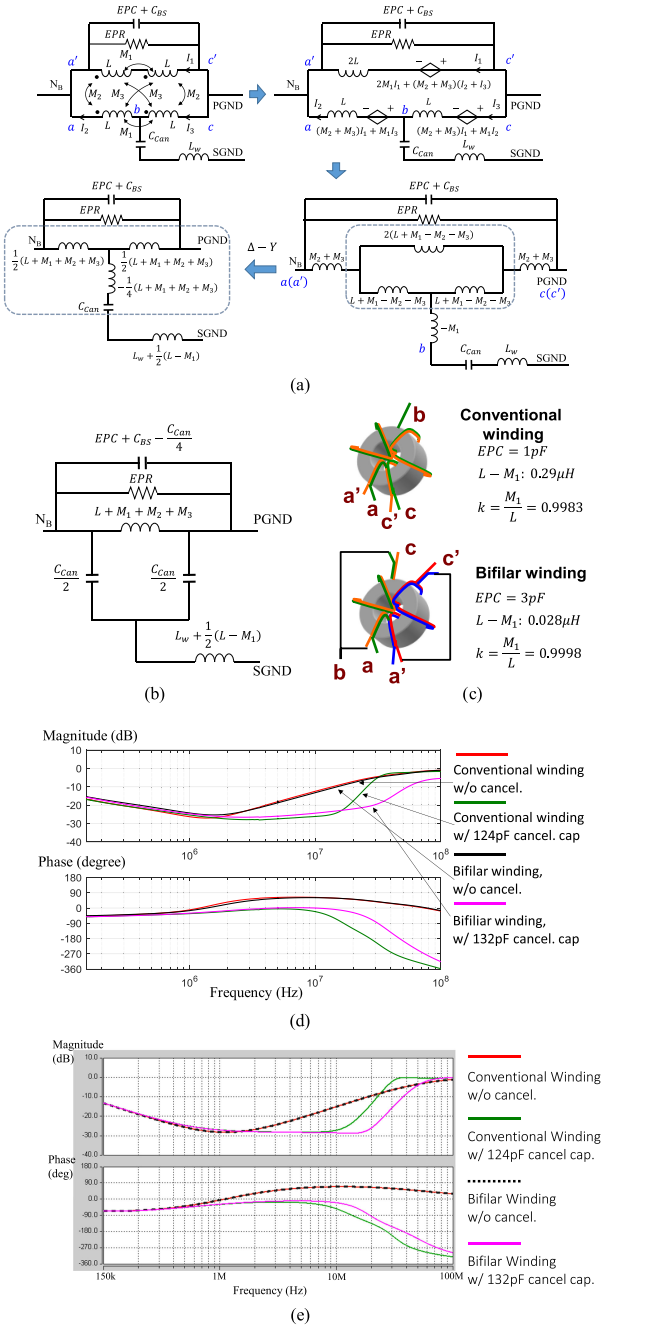

Fig. 19. Parasitic capacitance cancellation. (a) Circuit realization and analysis with mutual inductance decoupling. (b) Equivalent π model of (a). (c) Winding structures of parasitic capacitance cancellation. (d) Measured transfer gains w/ and w/o cancellation. (e) Simulated transfer gains w/ and w/o cancellation.

can be greatly improved. The comparison of the measured S21 with 50-Ω source and load impedances before and after applying the cancellation technique to these two winding structures is shown in Fig. 19(d). A simulation is also conducted in Saber to compare the transfer gains of the two cases in Fig. 19(e). Obviously, the effective frequency range of the bifilar structure is wider than that of the conventional winding. The simulation results in Fig. 19(e) match the measured results in Fig. 19(d).

The comparison of the measured CM noise with the original dc-bus filter, with copper shielding added in Fig. 14 and further with winding capacitance cancellation technique in Fig. 19 is

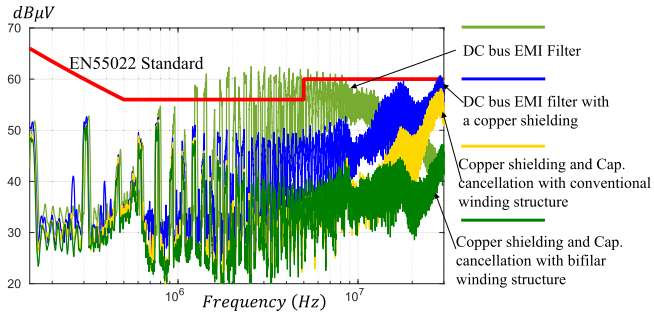

Fig. 20. Comparison of the measured CM noise.

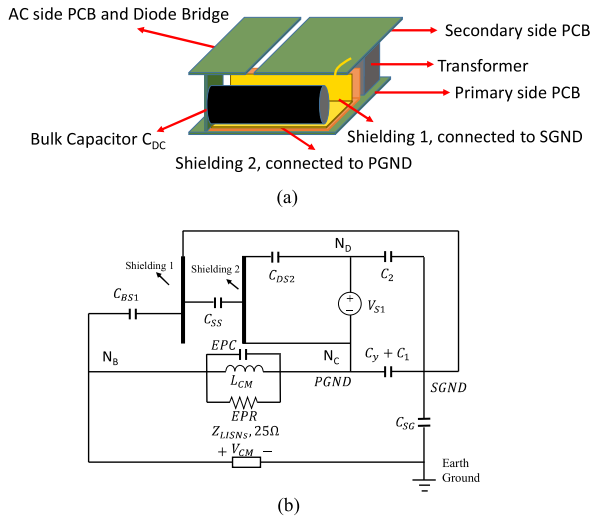

Fig. 21. (a) Physical realization of double shielding. (b) Equivalent circuit.

shown in Fig. 20. It is shown that, with the capacitance cancellation technique and the bifilar winding structure, HF CM EMI can be further reduced by up to 15 dB.

The advantage of the capacitance cancellation is that not only EPC but also the parasitic capacitance across the CM inductor is cancelled. The drawback is that since the cancellation capacitor is across PGND and SGND, it must meet safety requirements. Using one $C_{\mathrm{Can}} = 4(\mathrm{EPC} + C_{\mathrm{BS}})$ on one of the two fully coupled windings instead of using two $C_{\mathrm{Can}} = 2(\mathrm{EPC} + C_{\mathrm{BS}})$ on two fully coupled windings separately can improve safety (one capacitor's failure rate is lower than that of two capacitors) and reduce cost.

C. CM Noise Reduction With Double Shielding Technique

The single shielding technique in Fig. 14 can be further improved to reduce HF CM EMI with a double shielding technique in Fig. 21. In Fig. 21(a), shielding 1 is close to C_{DC} and connected to the SGND. Shielding 2 is under shielding 1 and above PCB PGND. It is connected to PGND and shields nodes N_C and N_D from shielding 1. The equivalent circuit is shown in Fig. 21(b). C_{BS1} is the parasitic capacitance between the node N_B, where C_{DC} is located, and shielding 1. C_{BS1} is connected to SGND via shielding 1. The measured C_{BS1} is 30 pF. C_{SS}, the parasitic capacitance between two shielding, was measured as 6.2 pF. C_{SS} is equivalently in parallel with $C_{\mathrm{y}} + \mathrm{C}_1$ and can be ignored because it is much smaller than $C_y + \mathrm{C}_1$. C_{DS2} is the

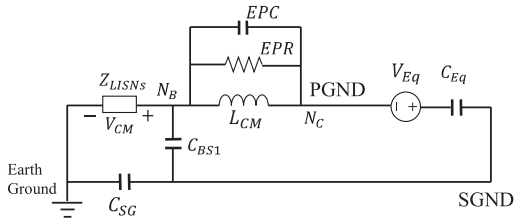

Fig. 22. Reduced CM equivalent circuit of an active clamp Flyback adapter with a dc-bus filter and double shielding technique.

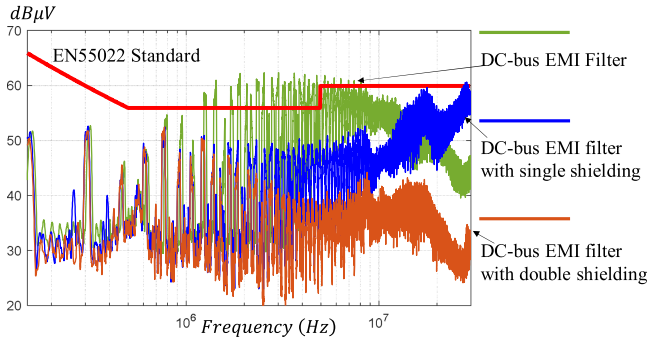

Fig. 23. Measured CM noise of an active clamp Flyback adapter with a dc-bus filter and double shielding technique.

parasitic capacitance between the node N_D and shielding 2 and it is in parallel with V_{S1}, so it can be ignored too.

The reduced equivalent circuit is shown in Fig. 22. As discussed previously, in Fig. 22, $C_{\rm SS}$ is ignored, and $C_{\rm BS1}$ work as part of the CM filter, which helps to reduce HF CM noise. The $C_{\rm BS}$ in Fig. 14 has been eliminated. And the voltage gain $\text{Gain}_{\rm DS}$ is given by the following equation, where $V_{\rm Eq}$ is defined in (1).

$$\text{Gain}_{\rm DS} = \frac{V_{\rm CM}}{V_{\rm Eq}} \approx \frac{Z_{\rm LISN} s C_{\rm SG}}{C_{\rm SG}+C_{\rm BS1}} \frac{s\left(C_{\rm SG}+C_{\rm BS1}\right)\left(\frac{sL_{\rm CM}}{\rm EPR}+1\right)}{s^2\left(C_{\rm SG}+C_{\rm BS1}\right)L_{\rm CM}+\frac{sL_{\rm CM}}{\rm EPR}+1}. \tag{10}$$

Based on Fig. 10, the impedance of the CM inductor is mostly dominated by EPR at high frequencies, so small EPC (1 pF) can be ignored in deriving (10) from Fig. 22. Comparing (8) and (10), both techniques have the similar performance. The only difference is $C_{\rm Can}/2$ in (8) is replaced with $C_{\rm BS1}$ in (10). Fig. 23 shows the comparison of the measured CM noise.

In Fig. 23, comparing with the single shielding technique, the double shielding technique can further reduce the HF CM noise above 2 MHz and meet the EMI standard because of the elimination of $C_{\rm BS}$ in single shielding implementation and the utilization of $C_{\rm BS1}$ as CM filter components. In this case, because 30-pF $C_{\rm BS1}$ is much larger than 10 pF $C_{\rm SG}$, based on Fig. 22, $C_{\rm BS1}$ has positive effects on the reduction of EMI.

The general rule of the shielding design is that its shape and size should cover the facing areas between the $C_{\rm DC}$ and PGND, between the $C_{\rm DC}$ and pulsating PCB traces, and between the $C_{\rm DC}$ and transformer windings. It should be noted that for safety reason, both copper shielding and the bulk capacitor $C_{\rm DC}$ should be covered with insulation tapes. The two shielding should have the same size and shape. The shielding performance is not susceptible to the distance between the capacitor and the shielding as long as the facing area mentioned previously is fully covered by the shielding and the distance between $C_{\rm DC}$ and the shielding is much smaller than the shielding size because the electric field fringing effect is minimized under that condition, which results in the minimized capacitive couplings between $C_{\rm DC}$ and PGND, between $C_{\rm DC}$ and pulsating PCB traces, and between $C_{\rm DC}$ and transformer windings.

It should be noted that for power adapters, typically a bridge rectifier is employed at the ac input. As analyzed previously, a dc-bus EMI filter helps to reduce the size and the power loss of the EMI filter. However, the effects of the capacitive coupling tends to be significant in the converter, so the techniques proposed in this article are applicable to general ac/dc adapters with a diode-bridge rectifier and a dc-bus filter.

V. Conclusion

In this article, the capacitive couplings within active clamp Flyback converters are investigated. The important capacitive couplings in an active clamp Flyback converter with dc-bus filter are first identified. The capacitive couplings are then extracted using a VNA. The CM noise model that includes capacitive couplings is developed. Based on the developed models, the effects of capacitive couplings on the CM EMI are analyzed. Techniques to reduce the CM noise due to capacitive couplings are developed. Experiments were conducted to validate the proposed theory and techniques. It is found that the electrolytic capacitor on the dc bus can significantly contribute to the capacitive couplings, and therefore, increase the CM noise in an active clamp Flyback converter with a dc-bus filter. Shielding and parasitic capacitance cancellation techniques are effective to reduce the CM EMI.

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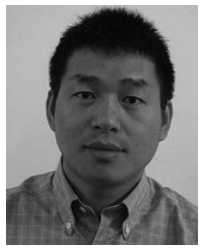

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